# Introduction

For this design there is chosen to create a combined traditional DAC, mixer and power amplifier (PA), because this leads to several advantages. One thing is that it results in a more compact solution. A compact solution allows the system to be faster, because there are less parasitic capacitances between the structures. Also the need of matching to 50 ohm between these structures becomes superfluous. Using such a combined system solution has a disadvantage that it is hard to generate high power, because power leakage generates heat which can damage the transistors. Moreover the use of large capacitors or inductors is not possible, because these require too much space to create in silicon. Normally they are placed on the PCB.

Such a solution could be useful for several systems. Mainly for systems that require high speed, low power or lack of sufficient available space for a PCB. One example for such a system is the WiFi connection in a mobile phone.

# System overview

The architecture of the system can be separated in several functional blocks: the DAC, mixer and amplifier.

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Whereby the DAC translates a 15 bit unary coded digital signal with a sample frequency of maximum 500MHz to an analogue signal. There is chosen for unary coding to increase linearity compared to binary coded signals. One of the reasons is that in the creation process of the transistors, it is more precise to make to transistors of the same size, than to make one with exactly two times the size.

The mixer works with a square wave, 2 GHz local oscillator (LO) frequency. The mixer can be divided in two types. The p-type and the n-type, where the p-type consist out of a flip-flop and a NAND and the n-type out of a flip-flop and a NOR.

The final functional block of this design, the amplifier, …

* System specs
  + 2 GHz carrier LO
  + Signal bandwidth 500MHz
  + Fs = 1GHz
  + Snr
  + IMD3 < 30 dBc
  + Sensitivity
  + Noise floor
  + Output power 20.97dBm
  + Output current 50mA
  + Output voltage swing
  + Efficiency
* Unary coding
  + 4 > 16 bit
* 2 directions of dac
  + Propotional to input level
* Level shifter
* 2 direction amplifier

# Results and analysis

The specified specifications are verified by the use of simulations. While providing a one tone signal, a transient measurement of the output power is simulated. This to verify a correct functioning DAC, that translates the digitals signals as supposed. This holds that the 15 bit digital unary code is translated to an analogue signal with 16 level resolution.

Next a DFT of the output voltage is simulated to see the spectral content of the one tone model. This to find the power of the harmonic distortion and the spurious-free dynamic range (SFDR). The SFDR describes the power of the fundamental signal to the strongest spurious signal at the output, which is most commonly the second harmonic.

Furthermore a two tone test is simulated, the two tone test is useful test the linearity of the DAC. Non-linear behaviour generates intermodulation products at the output of the DAC. The power of these intermodulation products will examined, especially the third intermodulation product (IM3). Because the IM3 frequencies are very close to the fundamental frequency (at 2f2-f1 and 2f1-f2), it is almost impossible to filter it out of the output signal; therefore, it is better to prevent creating them.

* + SNR = 20\*log(fundamental/[sqrt(sum(sqr(noise))])
  + SFDR = 20\* log(fundamental/3th harmonic)
  + THD = 20\*log(sqrt(sum(sqr(harmonics/fundamental)))

F\_LO = 2 GHz

512 periods

512\*500=256ns

F\_IF = 50MHz

T\_IF = 20ns

256ns/

Guidelines task 1: System level (application, architecture, test benches, signal levels, segmentation) and test benches Prepare test‐benches that simulate the time‐domain performance of the Power Mixing‐DAC. You can start with a system level ideal description (RTL – registry transfer level, i.e. a functional level), where the system is described by functions/blocks which communicate between each other. The functions can be: switched‐current sources, AND‐gate mixers, high‐speed latches. When this design operates properly, you can substitute the ideal‐description of the function with their transistor level implementation. This model should be simulated with transient simulations. The parameters should be chosen conveniently, so that FFT of the transient data can properly demonstrate the frequency domain performance.

To simulate a single‐tone you should choose the length of simulation in such a way that an integer period of the input signal frequency and the LO mixing signal are captured.   For fLO=2GHz, TLO=500ps. For example, we want to capture in our transient simulation 512 periods of the LO, i.e. 512\*500ps=256ns. For example, we want to simulate an input sinewave of about 45MHz (Tsig=22.22ns). How many periods will fit in 256ns? 11 full periods will fit in it. Hence, we fix the input frequency to 42.96875MHz (Tsig=23.2727(27)ns). This signal needs to be ideally digitized into 4 bits sampled with 1GSps clock. For the whole simulation you need to add some additional settling time, e.g. 10ns. Therefore, the whole transient simulation will be about 266ns. When you get time domain data of the output Mixing‐DAC signals, you need to calculate the spectrum. For that you need to call DFT and set the number of point (e.g. 32768), start and end time for the time data window, which should be 256ns. Choose start and end time in such a way that the values are close to each other. The fft results is an array of complex numbers that are associated with certain frequency bins. To get the power of the signal in the frequency domain, you need to calculate the absolute value of these complex numbers per frequency and take the power of it. Then, plot it in the logarithmic scale (with base 10). You can now see the LO signals, the signal and mirror bands and the main harmonic (2GHz ± 42.96875MHz), the harmonic distortion components (2GHz ± k\*42.96875MHz) and the noise floor. Calculate SFDR.

To simulate IMD3, you need a two tone test. Since you want to capture full periods in time domain in order to avoid frequency leakage in the FFT calculation, now you can work it out again backwards. The time window is again 256ns. We want to simulate, for example 11 full period of signal 1 and 14 full periods of signal 2. Hence, fsig1=42.96875MHz (Tsig1=23.2727(27)ns) and fsig2=54.6875MHz (Tsig2=18.2857ns). You can do FFT and see the spectrum.   For this task you need to model the ideal components with their proper voltage/current levels, output and input impedances, so that when you put the transistor level components the performance does not deteriorate much. For this task you need to lead the process of integration.

Task 2: System level (η=Psig/Ptot, power consumption, literature, speed, linearity IMD3/SFDR) and test benches; Compare efficiency vs other approaches (e.g. the project of group 1). What are the other options in terms of architectures for the power‐DAC. How do you compute the efficiency? What can you change to improve efficiency.